IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL NO:

In Re Application of: BONOMO, et al.

Confirmation No. 2397

Serial No. 09/677,314

Filed: September 29, 2000

For: METHOD AND SYSTEM FOR INCREASING CONTROL INFORMATION FROM GPIOS

APPELLANT'S BRIEF

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
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In Re Application of:	Date: February 13, 2004
BONOMO, et al.	Confirmation No. 2397
Serial No. 09/677,314	Group Art Unit: 2189
Filed: September 29, 2000	Examiner: Vo, Tim T.

For: METHOD AND SYSTEM FOR INCREASING CONTROL INFORMATION FROM GPIOS

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

APPELLANT'S BRIEF ON APPEAL

Sir:

Appellant herein files an Appeal Brief drafted in accordance with the provisions of 37 C.F.R. § 1.192(c) as follows:

I. REAL PARTY IN INTEREST

Appellant respectfully submits that the above-captioned application is assigned, in its entirety to International Business Machines Corporation, Armonk, New York.

II. RELATED APPEALS AND INTERFERENCES

Appellant states that, upon information and belief, he is not aware of any co-pending appeal or interference which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Application Serial No. 09/677,314 (the instant application) as originally filed included claims 1-20. Claims 1-8 and 10-20 are pending. In response to the Office Action dated 3/13/2003, Appellant canceled claim 9 and amended claim 10. The amendment to claim 10 merely corrected a grammatical error. Claims 1, 2, 3, 4, 5, 6, 7, 8, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, and 20 are on appeal and all applied prospective rejections concerning Claims 1, 2, 3, 4, 5, 6, 7, 8, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, and 20 are being appealed herein.

IV. STATUS OF AMENDMENT

All amendments made to the instant application have been entered.

V. SUMMARY OF THE INVENTION

The present invention provides for increasing control information from a single general purpose input/output (GPIO) mechanism. The aspects include utilizing a single GPIO mechanism with a socket on a computer system. Determinations of whether a first card, a second card, or no card is installed in the socket occur according to detected changes in signal states on a single signal line between the GPIO mechanism and the socket. Detection of a first state on the single signal line indicates presence of a first card in the socket, while detection of a second state on the single signal line indicates presence of a second card in the socket. Detection of a state change on the single signal line indicates no card presence in the socket, where the changes occur in response to signals sent by a POST to the GPIO mechanism.

Through the present invention, an increase in the amount of control/information that is available using GPIOs is achieved in a straightforward and effective manner without increasing the number of GPIOs. Further, trinary states on a single signal line are detectable quite readily with the inclusion of an R-C circuit on the single signal line.

VI. ISSUES

The issue presented is:

(1) whether claims 1-8 and 10-20 are each unpatentable under 35 U.S.C. 102(e) as being anticipated by Winston.

VII. GROUPING OF CLAIMS

Appellant hereby states that claims 1-8 and 10-20 form one group.

VIII. ARGUMENTS

A. Summary of the Applied Rejections

The final office action dated 11/4/03 rejected: claims 1-8 and 10-20 under 35 U.S.C. 102(e) as being anticipated by Winston. In making the rejection, the Examiner states:

> **As for claims 1, 10 and 17, Winston teaches a method for increasing control information from a single general purpose input/ouput (GPIO) mechanism (see figure 3, module detection unit 310 and column 4 line 50 to column 5 line 27, wherein the detection unit 310 detects card insertion for slot 103, 106), the method comprising:**
>
> **utilizing a single GPIO mechanism with a socket on a computer system (see figure 3, module detection unit 310, line 311 and column 4 line 50 to column 5 line 27, wherein the detection module monitors the present [sic] of card insertion in slots 103, 106 via line 311); and**
>
> **determining whether a first card, a second card, or no card is installed in the socket according to detected changes in signals state on a single line between the GPIO mechanism and the socket (see figure 3, module detection unit 310, line 311, module occupation signal, module 2 occupation signal and column 4 line 50 to column 5 line 27, wherein the detection generates module 1 and module 2 occupation signal correspondingly to the detection line 311. Further, figure 7, step 701 discloses if slots 103, 106 is [sic] occupied or not).** ...

Appellant respectfully requests that the Board reverse the Examiner's final rejection of the pending Claims.

B. The Cited Prior Art

Winston discloses that a computer system includes a bus. A first connector is coupled to the bus. A power lock-out unit is coupled to the first connector. The power

lock-out unit prevents a system power supply from receiving a power-on request when a first module is not coupled to the first connector.

C. **Claims 1-8 and 10-20 Are Not Unpatentable Under 35 U.S.C. 102(e)**

As recited in the independent claims 1, 10, and 17 of the present invention, a single general purpose input/output (GPIO) mechanism is utilized with a socket on a computer system, and detection of at least three separate conditions of the socket occurs based on a single signal line between the GPIO mechanism and the socket. Claim 1 further recites that detected changes in signal states on the single signal line between the GPIO mechanism and the socket determine whether a first card, a second card, or no card is installed in the socket. This ability to detect at least three states on a single signal line in the present invention increases the control information available from the GPIO mechanism.

The Examiner asserts that Winston uses a single detection line 311 with a module detection unit to determine module 1 and module 2 occupation signals for slot connectors of a computer system. Appellant respectfully points out that although Figure 3 of Winston illustrates line 311 as a single bi-directional arrow, Winston's description of Figure 3 indicates that "Line 311 in FIG. 3 illustrates a plurality of module detection connections that connects the module detection unit 310 to a plurality of slot connectors." (col. 4, lines 57-60, emphasis added)

Appellant further respectfully directs attention to Winston's Figure 6 which illustrates the module detection unit 310 and to its accompanying description in col. 7, lines 38-64. In this section of col. 7, Winston discloses that "the module detection unit

310 is connected to the first slot connector 103 and the second slot connector 106 via the module detection connections 311." (emphasis added) Winston further describes the plurality of module detection connections 311 shown in Figure 6 by teaching in lines 44-64 of col. 7:

> The module detection connections 311 include a first module detection connection 620 that connects the first pull-up resistor 610 to the first slot connector 103. The first module detection connection 620 transmits a MODULE1_OCCUPATION signal to the first slot connector 103. ... The first slot connector 103 returns a low signal on the first module detection connection 620 when the first slot connector 103 is occupied and returns a high signal when it is vacant. The module detection connections 311 include a second module detection connection 621 that connects the second pull-up resistor 611 to the second slot connector 106. The second module detection connection 621 transmits MODULE2_OCCUPATION signal to the second slot connector 106. ... The second slot connector 106 returns a low signal on the second module detection connection 621 when the second slot connector 106 is occupied and returns a high signal when it is vacant.

Thus, Appellant respectfully submits that Winston clearly teaches the use of a plurality of connection lines with a separate connection signal line for each slot connector. Each connection line transmits a separate high or low signal to indicate whether the slot to which it is connected is vacant or occupied. Thus, each of the plurality of signal lines is taught as being capable of indicating only two states for its corresponding socket. Appellant respectfully submits that such use of a plurality of connection signal lines to detect only two separate conditions for each of a plurality of sockets not only fails to teach or suggest the recited invention but teaches away from Appellant's recited invention, in which detection of at least three separate conditions of a socket (whether a first card, a second card, or no card is installed) occurs based on a single signal line between the GPIO mechanism and the socket.

In view of the foregoing, Appellant respectfully submits that independent claims 1, 10, and 17 are allowable over the cited art. Further, claims 2-8, 11-16, and 18-20 depend from one of the independent claims. Thus, these dependent claims include the features of the independent claims that are believed to be allowable over the cited art, while adding further features. Therefore, claims 2-8, 11-16, and 18-20 are also respectfully submitted as allowable over the cited art for at least those reasons stated hereinabove.

Accordingly, Appellant respectfully requests withdrawal of the rejection under 35 U.S.C. 102(e) and respectfully requests that the Board reverse the final rejection of Claims 1-8 and 10-20.

E. Summary of Arguments

For all the foregoing reasons, it is respectfully submitted that Claims 1, 2, 3, 4, 5, 6, 7, 8, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, and 20 (all the Claims presently in the application) are patentable for defining subject matter which would not have been unpatentable under 35 U.S.C. § 102(e). Thus, Appellant respectfully requests that the Board reverse the rejection of all the appealed Claims and find each of these Claims allowable.

Note: For convenience of detachment without disturbing the integrity of the remainder of pages of this Appeal Brief, Appellant's "APPENDIX" section is contained on separate sheets following the signatory portion of this Appeal Brief.

This Brief is being submitted in triplicate, and authorization for payment of the required Brief fee is contained in the transmittal letter for this Brief. Please charge any fee that may be necessary for the continued pendency of this application to Deposit Account No. 50-0563 (IBM Corporation)

Respectfully submitted,

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February 13, 2004
Date

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IX. APPENDIX

1. A method for increasing control information from a single general purpose input/output (GPIO) mechanism, the method comprising:

utilizing a single GPIO mechanism with a socket on a computer system; and

determining whether a first card, a second card, or no card is installed in the socket according to detected changes in signal states on a single signal line between the GPIO mechanism and the socket.

2. The method of claim 1 wherein determining further comprises writing a signal in a first state by a POST (power-on self test) routine to the GPIO mechanism.

3. The method of claim 2 wherein determining further comprises reading a state of the GPIO mechanism by the POST routine.

4. The method of claim 3 wherein determining further comprises writing the signal in a second state by the POST routine to the GPIO mechanism.

5. The method of claim 4 further comprising reading a state of the GPIO mechanism by the POST routine.

6. The method of claim 5 wherein when the state of the GPIO mechanism changes in accordance with state changes by the POST routine, no card is installed in the socket.

7. The method of claim 6 wherein when the state of the GPIO mechanism does not change, one of the first and second cards is installed.

8. The method of claim 7 wherein one of the first and second cards pulls-up the signal line, and the other of the first and second cards pulls-down the single signal line.

10. A system for increasing control information from a single general purpose input/output (GPIO) mechanism, the system comprising:

a computer system planar including a socket; and

a GPIO means coupled to the socket via a single signal line, wherein at least three states of occupancy of the socket are detected according to state changes on the single signal line.

11. The system of claim 10 wherein when a first card occupies the socket, the single signal line is pulled to a first logic state.

12. The system of claim 11 wherein when a second card occupies the socket, the single signal line is pulled to a second logic state.

13. The system of claim 12 wherein when no card occupies the socket, the single signal line changes state in response to state changes of a signal from a POST (power-on self test) routine.

14. The system of claim 13 further comprising a controller coupled to the GPIO to perform the POST routine.

15. The system of claim 14 further comprising a transient storage circuit coupled to the single signal line to assist in the detection of state changes.

16. The system of claim 15 wherein the transient storage circuit comprises a resistor-capacitor (R-C) circuit.

17. A method to allow trinary state determination from a single signal line, the method comprising:

providing a GPIO (general purpose input/output) mechanism for a socket on a computer system planar; and

utilizing a transient storage circuit on a signal line between the GPIO mechanism and the socket to allow detection of at least three separate conditions of the socket.

18. The method of claim 17 wherein utilizing a transient storage circuit further comprises utilizing an R-C (resistor-capacitor) circuit.

19. The method of claim 18 wherein utilizing an R-C circuit further comprises detecting a first state on the signal line indicating presence of a first card in the socket, detecting a second state on the signal line indicating presence of a second card in the socket, and detecting a state change on the signal line indicating no card presence in the socket.

20. The method of claim 19 wherein detecting the first state, the second state, and the state change further comprises detecting whether state of the signal line changes in response to signals sent by a POST (power-on self test) routine to the GPIO mechanism.